Exercise 6: Memory and memristor characterisation

Location: MED 2 1519

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1. Summary

In this exercise you will continue with the device characterization by working on floating gate transistors (FGFETs) based on MoS_2. These devices operate on the same principle as flash memory devices used in consumer electronic device today and are based on field effect transistors with an additional conductive island in the stack in which charges can be stored (more about this in the background section).

The main goal of this exercise is to carry out basic memory characterization, identifying the memory window and the influence of the programming state on the electrical conductance of the device. In the second part of the exercise, you will connect the FGFETs as memristors, two-terminal memory devices with an electrical resistance that depends on the previous current that passed through it.

2. Background

2.1. Floating gate transistor based on a 2D material

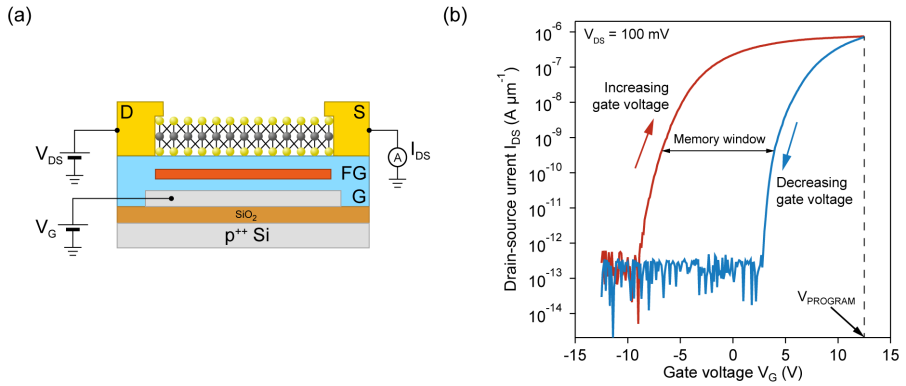


Figure 1. (a) Schematic of the MoS_2-based floating gate memory transistor. (b) Transfer characteristic of the floating-gate transistor (I_{DS} vs. V_G) acquired for two different gate voltage sweep directions. The variation of the threshold voltage V_{TH} is called the memory window, while the maximum voltage reached during the V_G sweep is the programming voltage $V_{PROGRAM}$.

The atomic scale thickness and high on/off ratio of transistors makes two-dimensional materials such as MoS_2 appealing for the fabrication of transistors with ultrashort channels and related structures such as floating-gate field effect transistors which can be used as memory elements. The structure of a FGFET based on a 2D material is shown on Figure 1a. It is based on a field-effect transistor, with an additional structure, the floating gate, placed between the channel and the gate, in this case also sometimes referrer to as the control gate. Depending on the voltage configuration of the device, charges can tunnel between the channel and the floating gate. The presence of charges on the floating gate will modify the response of the transistor so that this effect can be used for the memory function. Flash memory devices, currently in

widespread use in consumer electronics is based on this same type of a structure and principle of operation. The relative simplicity of their structure makes them attractive. The use of 2D materials for the channel instead of Si brings the possibility of aggressive scaling beyond 12 nm and in the same time also increase device reliability thanks to the atomic scale thickness as well as reduced cell-to-cell interference between neighbouring thin film floating gates in FGFETs.

The memory effect can be most easily observed by performing a gate voltage (V_G) sweep, resulting in a transfer characteristic shown on Figure 1b. As the voltage is increased from a low value, we get a standard response for an n-type transistor except that the current follows a different curve as the voltage is decreased. The difference between the threshold voltages in the two sweep directions is referred to as the memory window, while the maximal voltage reached during the voltage sweep is the programming voltage, $V_{PROGRAM}$.

The hysteresis in the transfer characteristic is a sign of charge trapping. It could also occur in other parts of devices, for example due to adsorbed water on the surface of the 2D materials. However, the magnitude of hysteresis is lower than in the case of charge trapping on the floating gate and such interfacial charge trapping is not reliable and repeatable enough to be used for implementing the memory function in practical devices. In order to minimize the memory effect from interfacial charge trapping, the devices used in this exercise have been passivated using a layer of resist which reduced the adsorption of water and oxygen on the MoS_2 channel which would be normally exposed.

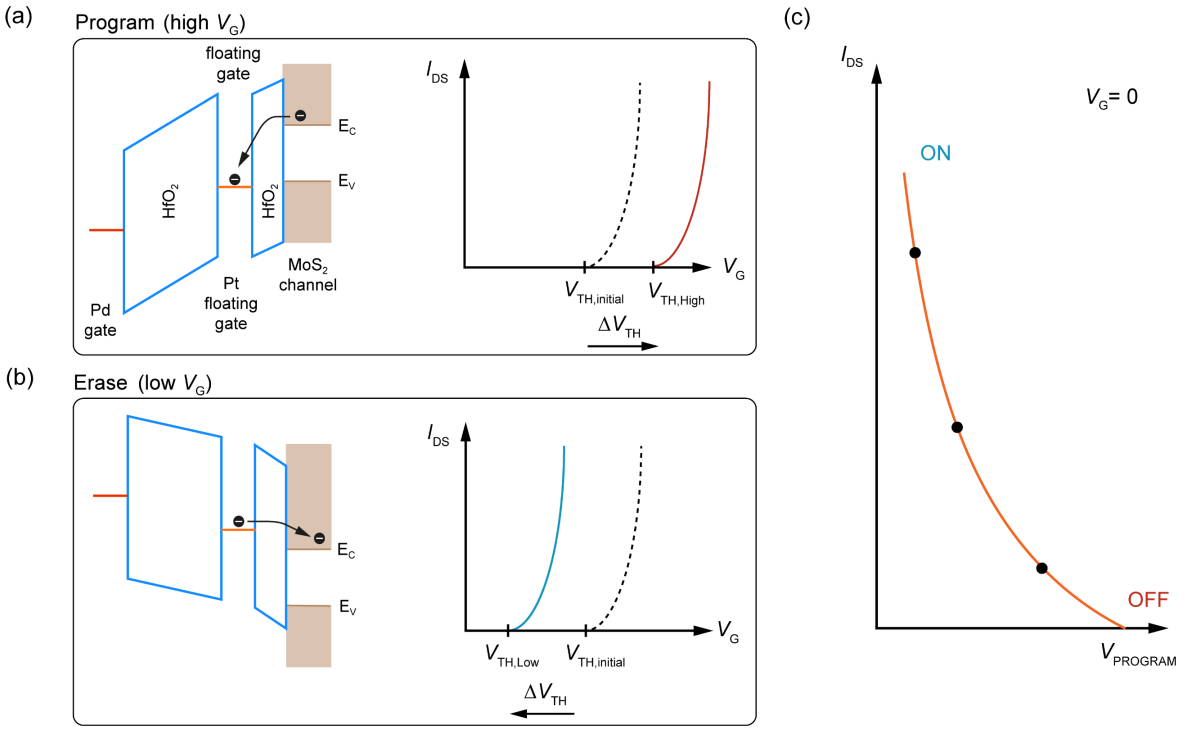


Figure 2. (a) Device band diagrams for the program and erase states of operation. (b) Device current for a "safe" value of a gate voltage (gate voltage value which is not expected to result in reprogramming of the memory, in this case V_G=0) depends on the value of the programming voltage that was previously applied to the gate terminal. We can use this effect to program different values of conductivities into the device.

We can program and erase the FGFET memory state by applying different values of voltages to the gate which leads to Fowler-Nordheim tunnelling of charges between MoS_2 and the floating gate. The tunnelling probability can be modulated by shifting the Fermi level of the semiconductor by the gate electric field. Applying a high, positive gate voltage (with a value

equal to $V_{PROGRAM}$), Figure 2a, results in electron injection into the floating gate and a shift of the characteristic to the right due to an increased threshold voltage, since an extra gate voltage now needs to be applied to overcome the electrostatic doping of the channel due to the electrons trapped on the floating gate. Similarly, applying a low voltage to the gate, Figure 2b, erases the memory state by casing electrons to tunnel from the floating gate back to the channel. For intermediate gate voltages, such as for example $V_G = 0V$ the band offsets between the floating gate and MoS_2 are such that tunneling of charges between the two is not very likely and the memory state is stable over longer periods of time (sometimes estimated to be on the order of 10 years for two memory states).

The amount of the charge injected into the floating gate during the programming operation depends on the value of $V_{PROGRAM}$. We can use this effect to program different values of conductivities into the device, Figure 2b, which can be read while applying a safe value of V_G (one which is not expected to reprogram the memory state) to the device.

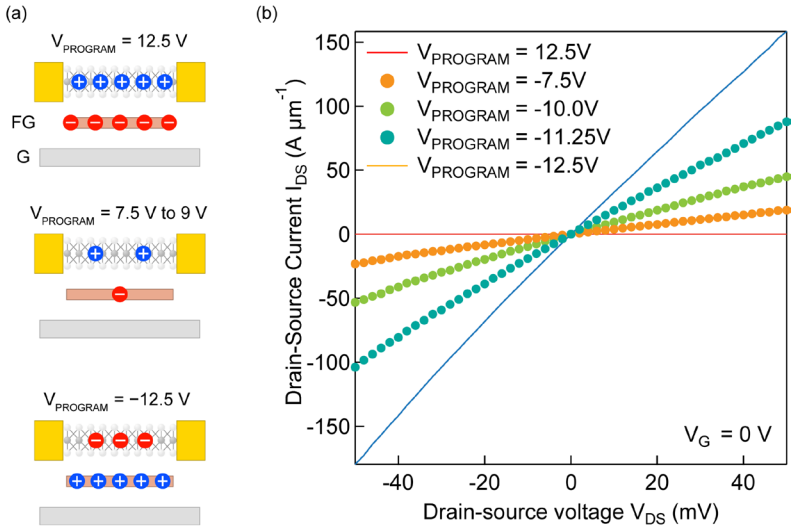


Figure 3. (a) schematic drawing of charges stored on the floating gate for different values of $V_{PROGRAM}$, resulting in additional electrostatic doping of the channel. (b) Biasing curves recorded for different programing states of the device.

This can be more clearly seen on Figure 3, where we show on panel a different charge configurations programmed into the device and on panel b the resulting biasing curves. For high values of $V_{PROGRAM}$ we inject a relatively larger amount of electrons into the floating gate and these charges induce opposite charges in the channel. Since the channel is made of an n-type material, the conductivity of the channel is reduced. The presence of electrons on the floating gate also makes the device less sensitive to the voltage applied to the gate voltage. For extreme values of $V_{PROGRAM}$ the device can even be programmed into an "always OFF" state, in which the gate voltage is fully screened by the charges in the gate and the device cannot be turned on. This is however valid only for the range of gate voltages that do not cause the memory state to be reprogrammed.

Similarly, for large negative $V_{PROGRAM}$, the floating gate is depleted of electrons and the device can be eventually programmed into an "always ON" state.

2.2. Memristors

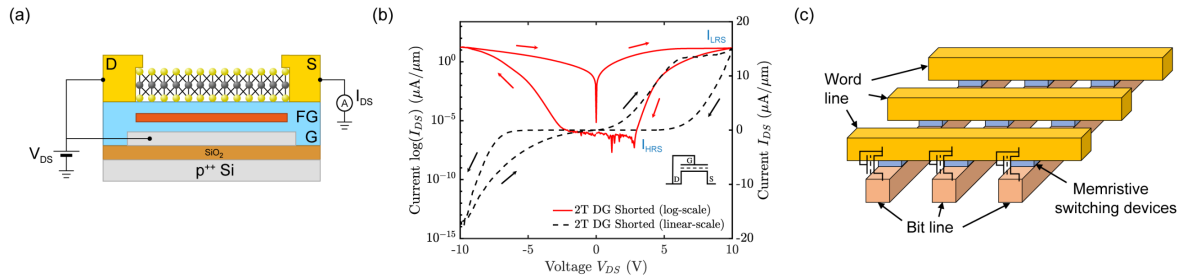


Figure 4. (a) MoS_2-based floating gate transistor connected in the memristor configuration. (b) biasing characteristic of the MoS_2 memristor. (c) Crossbar array with perpendicular nanowires BL and WL with memristive devices at the crossing points. Source: Asmund Ottesen, master thesis, EPFL.

The floating gate transistors are by nature three-terminal devices (source, drain, gate). By connecting source or drain electrode with the gate, they can be converted into memristors, a two-terminal device with an electrical resistance that depends on the device's history.

2.3. Wire bonding and packaging (repeated from Exercise 5)

In order to connect the contact pads on the devices with the external electronics, the TA used the method called wire bonding and a wire bonder, Figure 5a. This is a common method for connecting integrated circuits to packages such as the one used in this exercise and shown on Figure 5b.

The wires used to make the connection have a diameter of 25 µm (for comparison, a typical diameter of a single hair is ≈ 80-100 µm) and are made of an alloy of aluminum and silicon (1%). During the wire bonding process, the user manipulates the tool wedge under a microscope. This wedge resembles a needle in a sewing machine with the thin wire in place of a thread. The hand motion of the operator is de-multiplied by a factor of 10, so that regular movements of the hand can be used to manipulate the tool under the microscope with sufficient precision. Once the sensor inside the tool detects mechanical contact with a contact pad, a short ultrasonic pulse is emitted which bonds the wire with the contact pad either on the chip or the package. The process is quite straightforward but requires some skill since a common beginner mistake is to apply too much pressure on the tip which can result in the failure of the insulating film under the contact pads and an electrical short circuit between the source/drain electrodes and the gate.

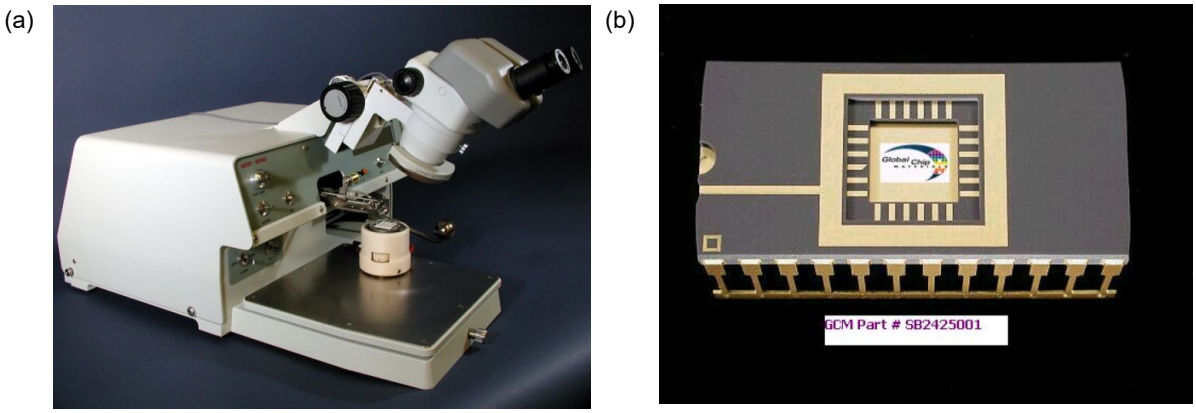


Figure 5. (a) Photo of a manual wire bonder from the company Westbond, used for preparing the chip using in this exercise. (b) Ceramic (mostly) chip package made by the company Kyocera, used in this exercise.

2.4. Electrostatic discharge (repeated from Exercise 5)

Electrostatic discharge (ESD) is an event in which static electricity from for example your clothes can be released. ESD can destroy delicate electronic devices such as the ones used in this and subsequent exercises. You have probably been zapped by such discharges when removing clothes for example. Such discharges involve potentials on the order of 100 V or even more (but the amount of charge is small so you do not get electrocuted). Smaller events, on the order of 10 V happen quite often but are normally not perceived. Those are still sufficient for destroying the devices by for example touching the chip with bare hands. Common methods or protection involve grounding equipment or yourself through a ~ 1MΩ which decreases the currents associated with ESD but allows the efficient removal of charges.

In order to protect the devices from ESD, you will need to take several precautions. You will attach an antistatic wristband, which will effectively ground you. It then advised to handle the chips, wires, electrical cabling etc. with the hand on which you are wearing the bracelet. The work area is also going to have a grounded mat and the chip is also stored in an ESD-safe box, made of a conducting polymer.

2.5. Description of the equipment used (repeated from exercise 5)

Keithley 2636B Sourcemeter

Figure 6. Front (left) and back (right) views of the Keithley 2636B 2-channel low-current sourcemeter.

The Model 2635B Sourcemeter from Keithley, a so-called source-measure unit (SMU instrument), combines high quality sources of current and voltage with precise measurements of the same, so that in a single channel you can for example apply a voltage and measure the current in the same time. The wide range of 1.5A DC, 10A pulse, 200V output (which we will not fully take advantage of here for safety reasons) and 0.1fA measurement resolution makes it ideal to test a wide range of lower current devices and materials. The Model 2635B has 6½-digit resolution, USB 2.0, ethernet and GPIB connectivity.

The instrument is connected to test fixtures using triaxial cables, in order to allow the high precision measurements of low currents.

Breakout box - test fixture

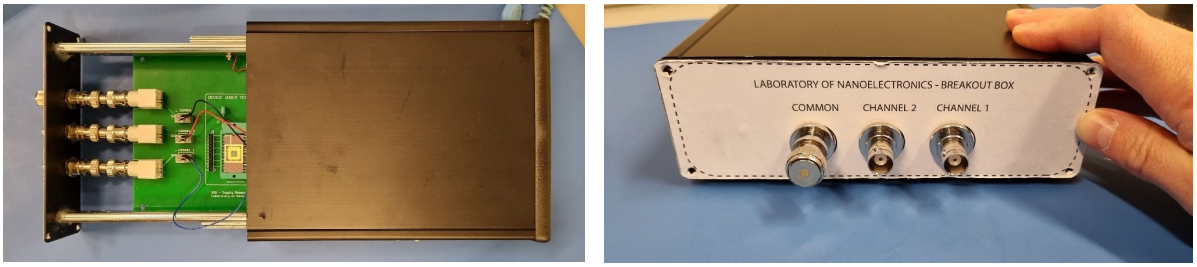
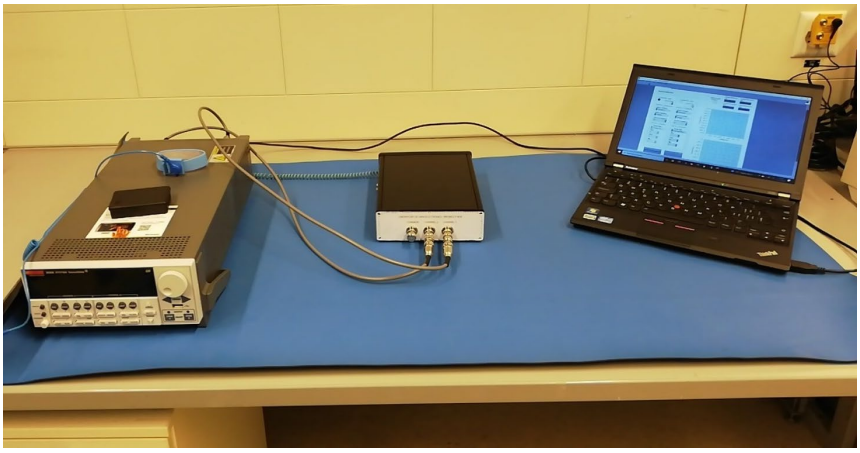


Figure 7. Top (left) and side (right) view of the breakout box that will be used in this exercise.

During the measurements, the chip with the mounted devices is kept in a breakout box whish allows interfacing the device with the measurement instrument. This box allows easily accessing the different contacts on the device and provides shielding from electromagnetic interference and light. On the front of the breakout box, we have three coaxial connectors which are connected to triaxial cables using adapters that leave the guard terminal floating. Channel 1 and 2 can be connected to the device terminal as well as the "Common" terminal which is connected to the reference terminal of the device and is connected to the shield of the triaxial cable using a grounding cap and closing the electrical circuit for measurements. The chip is placed into a ZIF (zero insertion force) socked on the board of the test fixture.

3. Description of experiments and tasks

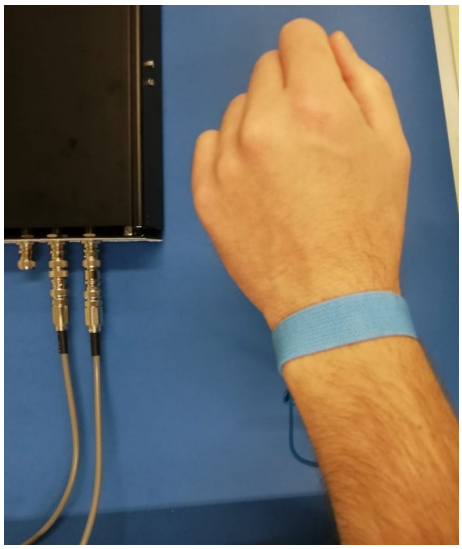
Following is the overview of the tasks and operations to be carried out in this exercise. The main goal is to perform electrical characterization of MoS_2-based floating gate devices operating as memories and memristors. Most of this description is identical to the analogous



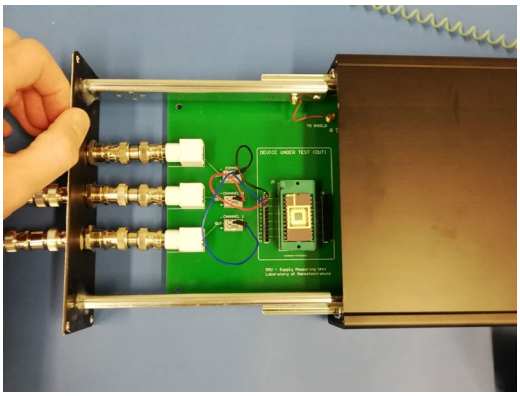
parts in exercise 5 (after all, these are similar devices but the application is different. The most important new element is step 5 in section 3.2, highlighted in yellow.

3.2. Setup – initial loading and handling of the chip with the device

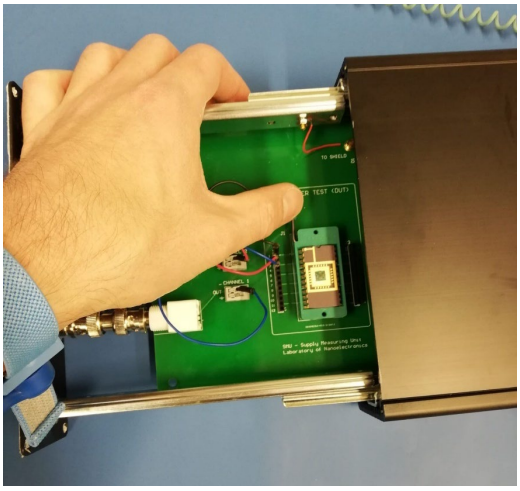
1. Ground yourself using the ESD Bracelet



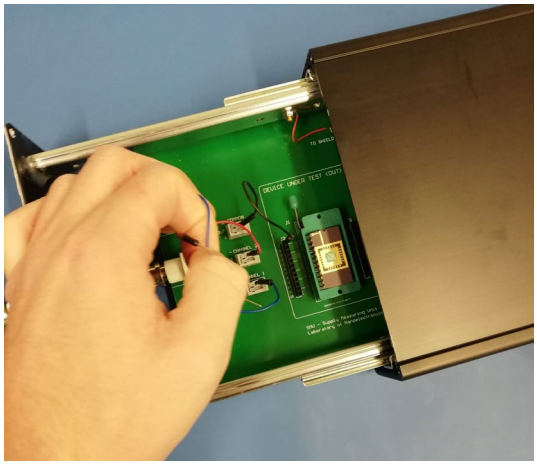
2. Open the breakout box and insert the device



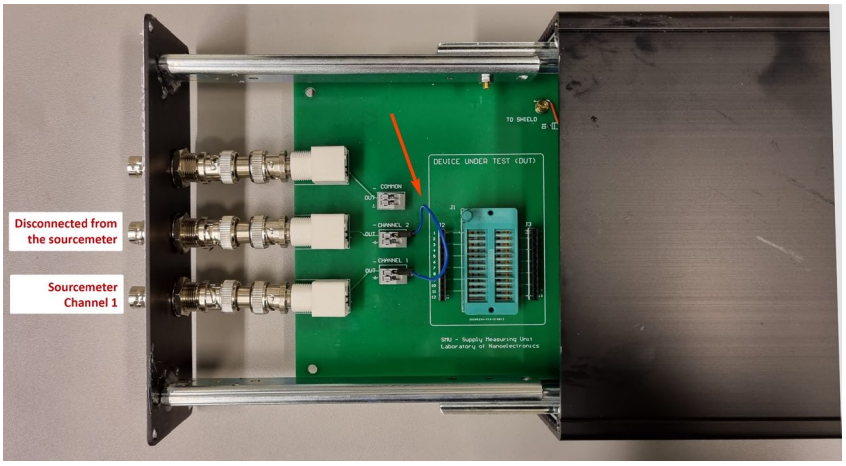
3. Change the lever position on the ZIF socket to lock the device in place



4. Connect the jumpers to the pins corresponding to the chip legs that you would like to access.



5. In order to configure the floating-gate transistors for memristor mode operation, disconnect first the channel 2 input on the breakout box from the sourcemeter. Inside the box, connect the channel 1 and channel 2 jumper terminals using one of the wires, as shown on the picture (red arrow). As a result, you will now be able to apply the same voltage to the drain and gate terminals of the desired FGFET.



3.3. Connecting an individual memory device

The chip contains four floating gate transistors (FGFETs) outlined on Figure 8 with contact pad numbers corresponding to the legs on the chip carrier and the pins in the breakout box.

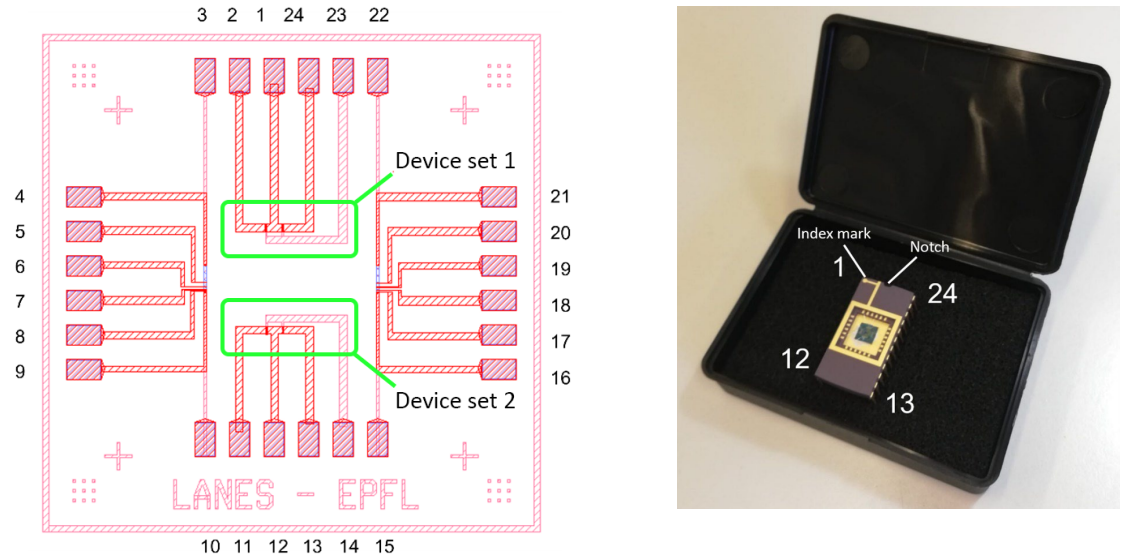


Figure 8. Left: schematic drawing of the device layout, with the corresponding pin numbering. There are two sets of memory (FGFET) devices. Device set 1 has the local back-gate connected to pin 23. Pins 2, 1, 24 correspond to electrical contacts. Device set 2 has the local back-gate connected to pin 14. Pins 11, 12, 13 correspond to electrical contacts that can be used as drain and source electrodes. Right: photograph of a chip carrier package. The pins are numbered in a counter-clockwise direction, starting from pin 1 at the index mark (rectangle close to a corner of the chip).

By manually connecting the wires between the jumpers and the pins you can access the different devices on the chip.

The dimensions of the transistors in the TLM device set 2 are shown in Figure 9, device set 1 has the same dimensions.

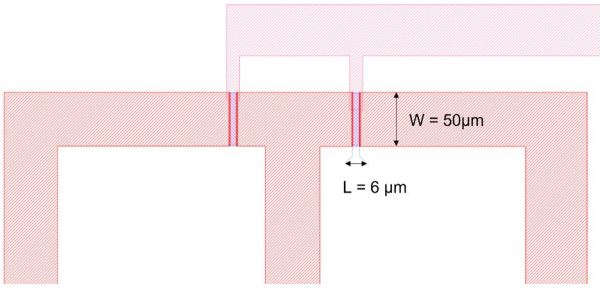


Figure 9. Channel dimensions for the FGFETs in the device set 2. Both FGFET device sets (1 and 2) have the same dimensions.

3.4. Familiarize yourself with the software interface (repeated from Exercise 5)

We will use a program in Labview for controlling the sourcemeter and measurement acquisition, with the interface shown in Figure 10.

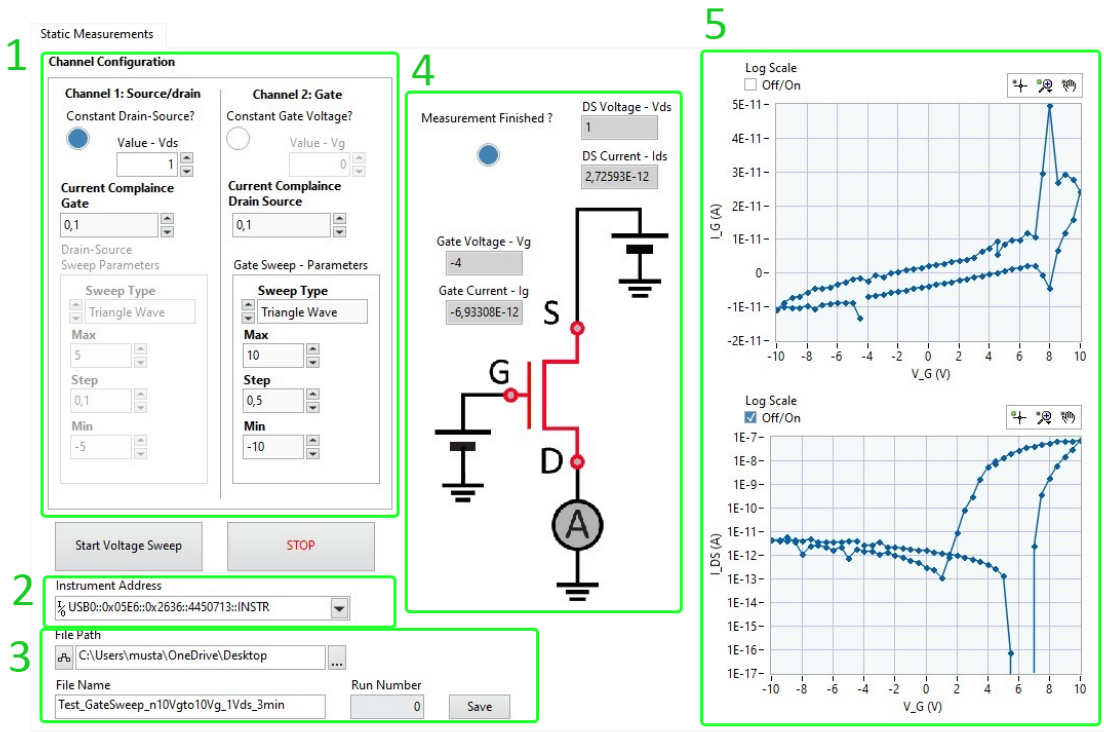


Figure 10. Interface for the data acquisition software used in this exercise.

Its main parts are:

1. Channel configuration
2. Instrument address
3. Path for saving the data
4. Schematic overview of the device and latest measurement values, together with an indicator showing if the current measurement has finished
5. Graphs with values from the current-voltage sweeps

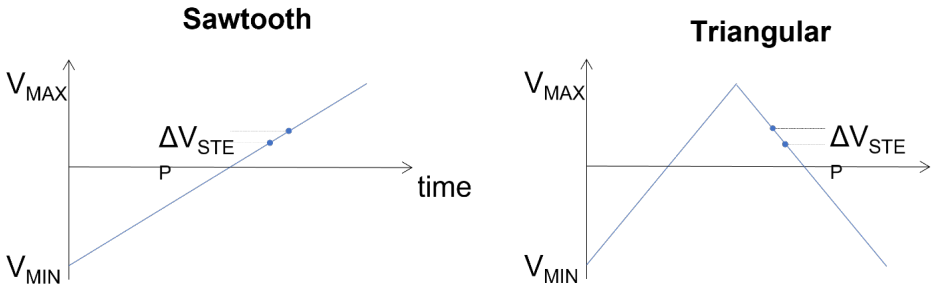
Configuring the instrument addres and file path

Scroll and select the first address and file path (folder in which want to save the file), enter a filename. To avoid overwritting a previously saved file, each time a file is saved, the run number is incremented and added to the end of the filename.

Configuring the voltage sweep

Here you can select the sweep type.

You can perform 2 types of sweeps, sawtooth or triangular:



When the configurations are ready, press Start Voltage Sweep. Stop will halt the software.

3.5. Perform device characterisation

1. **Memory window measurement.** For one of the FGFETs, set the bias voltage to V_{DS} = 100 mV and cycle the gate voltage V_G in the -10V , 10V range while recording I_{DS} vs V_G. How big is the memory window using constant current method for extracting the threshold voltage values?
2. **Programming different conductance values.** Start by erasing the previous state by performing a partial gate sweep (sawtooth sweep), to V_{RESET} (-10V). Next, Program the memory to V_{PROG} by performing a partial gate sweep (sawtooth sweep), up to the desired V_{PROG}. Once the V_{PROG} value has been reached on the gate terminal, set the gate reading voltage to V_{GS} = 0. Perform a bias ($I_{DS}-V_{DS}$) sweep. Repeat for V_{PROG} = 4, 6, 8, 10V. How does the device conductance depend on the V_{PROG}?
3. **Memristor operation.** Connect the same device into the memristor configuration. Perform a full voltage sweep cycle (triangular sweep) within the following ranges: V_{DS}= ±2 V, ±4 V, ±6 V, ±8 V, ±10 V. How does the ratio of I_{LRS}/I_{HRS} (see definition on Figure 4) depend on the programming voltage?

4. Questions for the report

In the report, please show and discuss the following:

1. A set of memory transfer characteristics showing the memory window.
2. Dependence of the device conductivity on the programming voltage.
3. Biasing curve for memristor operation and I_{LRS}/I_{HRS} values and their dependence on the magnitude of the voltage sweep